8 Channel CMOS logic to High-Voltage Level Translator

Preliminary Technical Data

ADG3123

FEATURES

2.3V to 5.5V input range
Output levels of -10V to +30V
High Current Carrying Capability:
10mA Continuous Current/channel
20mA Peak Current/channel
Rise /Fall time: 200ns typical
Propagation delay : 100ns Typical
20 lead TSSOP package in Pb-free

APPLICATIONS

Low voltage to high-voltage Translation
TFT-LCD panels
Piezoelectric Motor driver for Camera Phones

FUNCTIONAL BLOCK DIAGRAM

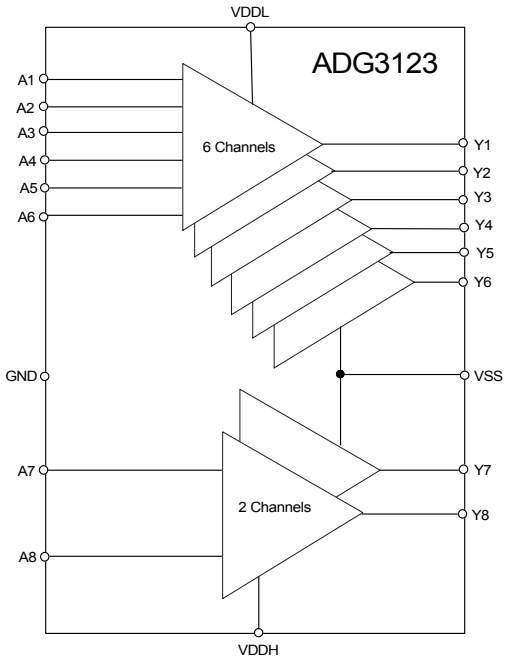

Figure 1

GENERAL DESCRIPTION

The ADG3123 is an 8-channel CMOS to High-Voltage level translator. It is fabricated on an enhanced LC²MOS process, giving an increased signal range, and ultra-low power dissipation.

The device translates the low voltage logic levels applied to the Ax pins to high voltage logic levels available at the Yx outputs. A LOW logic present at the Ax inputs will switch all outputs to the VSS rail. When a HIGH logic level is applied, the outputs will be switched to VDDL supply rail for Y1 to Y6 and VDDH for Y7 and Y8. For normal operation the VDDL≤VDDL conditions should always be met.

The output stages are optimized to drive capacitive loads ensuring fast rise and fall times that makes the ADG3123 an ideal driver for TFT-LCD panel applications.

The ADG3123 is guaranteed to operate over the -40°C to +85°C temperature range and is available is a compact 20 lead TSSOP Pb-free package.

PRODUCT HIGHLIGHTS

1. 2.3V to 5.5V input signal range
2. Output voltage levels of -10V to +30V
3. High current carrying capability.
4. Fast rise/fall times :200ns typical
5. Compact 20 lead TSSOP Pb-free package.

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SPECIFICATIONS

V_{DDH} = V_{DDL} = +27V to +30 V, V_{SS} = −7V to -10 V, VAx = 2.3V to 5.5V; GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
DIGITAL INPUTS (Ax)				
Input High Voltage, V_{IH}		2	V min	VAx = 3V to 5.5V
		1.7	V min	VAx = 2.3V to 2.7V
Input Low Voltage, V_{IL}		0.8	V max	VAx = 3V to 5.5V
		0.7	V max	VAx = 2.3V to 2.7V
Input Current I_{IL} or I_{IH}	±1		µA typ	V_{IN} = 0 V or V_{DD}
		±5	µA max	
Capacitance, C_I	5		pF typ	
DIGITAL Outputs (Yx)				
Output High Voltage, V_{OH}		V_{DDX} − 1	V min	I_{OH} = -100uA
Output Low Voltage, V_{OL}		V_{SS} + 1	V max	I_{OL} = +100uA
Output impedance, R_o	20		Ω typ	
SWITCHING CHARACTERISTICS[3]				Figure 2
Propagation Delay	100		ns typ	
Rise Time	200		ns typ	
Fall Time	200		ns typ	
Operating frequency	20		KHz typ	
Channel-to-Channel Skew	TBD		ns typ	
Part-to-Part Skew	TBD		ns typ	
POWER REQUIREMENTS				Digital inputs = 0V or VDD_X, No load
I_{DDL}	3		µA typ	
		TBD	µA max	
I_{DDH}	1		µA typ	
		TBD	µA max	
I_{SS}	10		µA typ	
		50	µA max	

[1] Temperature range is as follows: B version: −40°C to +85°C.

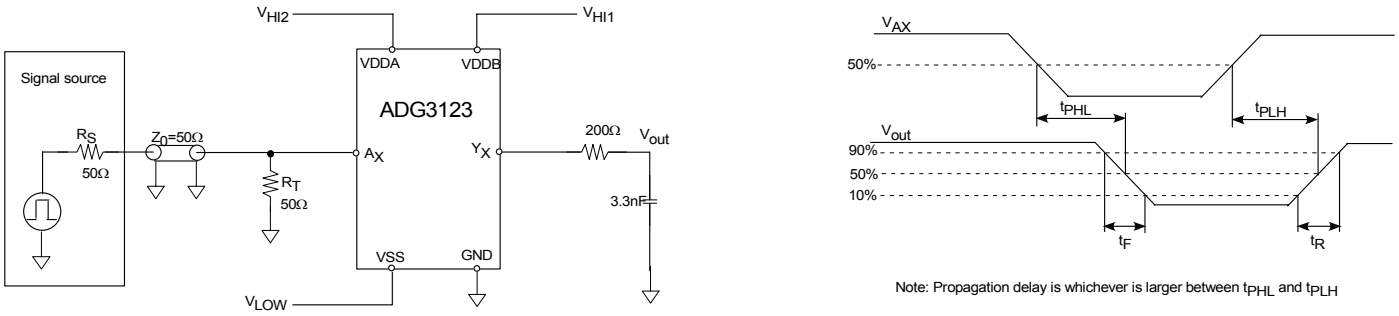

Figure 2. Switching characteristics test circuit

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 2.

Parameter	Min
V_{DD} to V_{SS}	+44 V
V_{DD} to GND	−0.3 V to +32 V
V_{SS} to GND	+0.3 V to −32 V
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DDX} + 0.3 V or 20 mA, whichever occurs first
Continuous Current, S or D	10 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Junction Temperature	150°C
θ_{JA}, Thermal Impedance	
TSSOP Package	143°C/W
Reflow Soldering (Pb-free)	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltage at IN, S, or D is clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

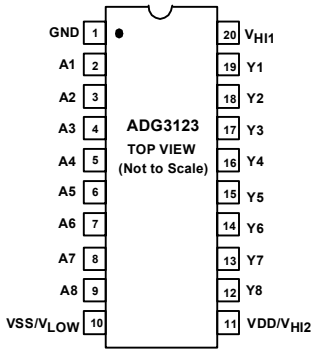

Figure 3. TSSOP Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground (0 V) Reference.
2, 3, 4, 5, 6, 7, 8, 9	A1, A2, A3, A4, A5, A6, A7, A8	Level Shifter Inputs. Voltage range 2.3V to 5.5V
10	V_{SS}	Most Negative Power Supply Potential in Dual Supplies (output low level for all outputs Y1 to Y8).
11	$V_{DDH"}$	Positive Power Supply used to provide the output high level for outputs Y7 and Y8.
12, 13, 14, 15, 16, 17, 18, 19	Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8	Level Shifter Outputs.
20	V_{DDL}	Positive Power Supply used to provide the output high level for outputs Y1 and Y6 ($V_{DDH} \geq V_{DDL}$).

TERMINOLOGY

Table 3.

Symbol	Description
V_{IH}	Logic input high voltage at Pin A1 to A8.
V_{IL}	Logic input low voltage at Pin A1 to A8.
V_{OH}	Logic output high voltage at Pin Y1 to Y8.
V_{OL}	Logic output low voltage at Pin Y1 to Y8.
R_o	Output impedance.
C_I	Capacitance at Pin A1 to A8.
I_L	Leakage current at Pin A1 to A8 when high.
I_H	Leakage current at Pin Y1 to Y8 when low.
Propagation delay	Propagation delay through the part from Ax to Yx.
Rise Time	Rise time of the output signal at Yx.
Fall Time	Fall time of the output signal at Yx.
Operating frequency	Frequency of the signal passed through the ADG3123.
Channel-to-channel skew	Propagation delay skew between any two channels on the device.
Part-to-Part skew	Difference between propagation delay on the same channel from different devices.
V_{DD}	Power supply voltage at Pin V_{DDH}/V_{DDL}.
V_{SS}	Power supply voltage at Pin V_{SS}.
I_{DD}	Supply current at the V_{DDH}/V_{DDL} pin.
I_{SS}	Supply current at the V_{SS} pin.

THEORY OF OPERATION

The ADG3123 is an 8-channel level translator capable of translating low voltage logic levels applied to its inputs (e.g. LVTTL, CMOS,) to high voltage logic levels. The device supports dual supply operation providing a negative output voltage for an input LOW logic level and a positive output voltage for an input HIGH logic level.

The ADG3123 requires three supply voltages VDDH, VDDL and VSS. The VDDL supply voltage sets the HIGH output voltage for outputs Y1 to Y6 while VDDH sets the HIGH outputs voltage for Y7 and Y8. The VSS supply sets the output voltage for all eight channels of the device. This configuration provides a high degree of flexibility which combined with low power consumption and small package makes the ADG3123 an ideal driver for TFT-LCD applications.

INPUT DRIVING REQUIREMENTS

The ADG3123 exhibits low input capacitance and leakage current. This reduces the load for the driver to a minimum allowing proper operation with any TTL/LVTTL or CMOS compatible drivers.

OUTPUT LOAD REQUIREMENTS

The low output impedance enables the ADG3123 to generate fast rise and fall times even into significant capacitive loads. If slower edge speeds are required, a resistor should be added in series with each output. During operation, the junction temperature must be kept below the absolute maximum rating value of 150^0C. The junction temperature can be calculated using the following formula:

$$\theta_J = \theta_{AMB} + \theta_{JA} \times \sum_i P_i$$

Where:

Θ_J = the junction temperature in degree Celsius;

Θ_{AMB} = ambient temperature in degree Celsius;

$\Theta_{JA}=143^0$C/W;

P_i = the power dissipated on each channel in Watt.

The power dissipated on each channel of the ADG3123 can be calculated using the formula shown below:

$$P_i = F \times C_L \times (VDD_X - VSS)^2$$

Where:

F= the frequency of the signal applied to the channel in Hz;

C_L = the load capacitance for the channel in F;

VDD_X = VDDL for Y1 to Y6 and VDDH for Y7 and Y8.

POWER SUPPLIES

For proper operation of the ADG3123, the voltage applied to the VDDH pin must always be greater than or equal to VDDL. Care must be taken to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the device being subjected to stresses beyond those specified under the Absolute Maximum Rating section. The recommended power supply sequence is as follows: turn VDDH on first followed by VSS and VDDL. The logic signals can then be applied to the device's inputs.

For optimum performance the VDDH, VDDL and VSS pins should be decoupled to GND as close as possible to the device.

APPLICATIONS

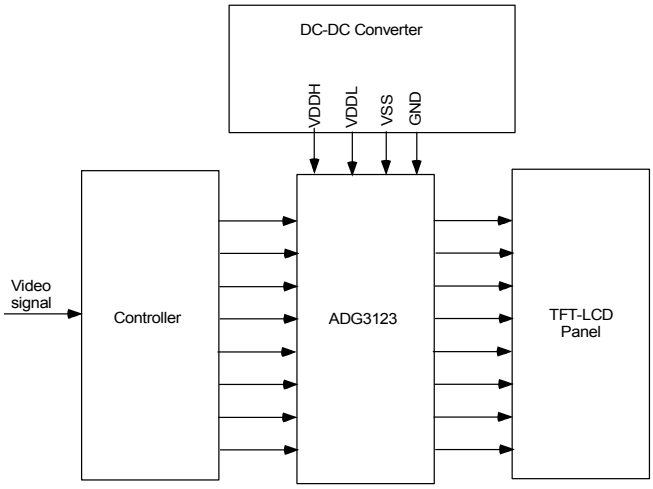

Figure4. Application diagram

OUTLINE DIMENSIONS

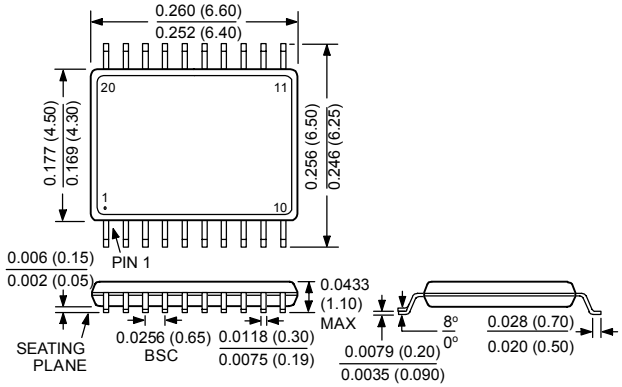

Figure 4. 20-LeadThin Shrink Small Outline Package(TSSOP)
RU-20
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3123BRUZ[1]	−40°C to +85°C	20-Lead Thin Shrink Outline Package (TSSOP)	RU-20

1. Z = Pb-free part

PR05655-0-7/05(PrF)

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